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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
08/654,760	05/29/1996	MADHUKAR B. VORA	V&F-001	7867

7590 08/01/2002

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EXAMINER

CRANE, SARA W

ART UNIT	PAPER NUMBER
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2811

DATE MAILED: 08/01/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

08/654,760

Applicant(s)

VORA, MADHUKAR B.

Examiner

Sara W. Crane

Art Unit

2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 12 April 2002.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-5 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-5 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 112

Claims 1-5 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Each of the independent claims uses the word "overlie" or "overlying," and it is not clear what Applicant means by this language. Note claim 1, lines 10-11, which states that the "floating gate" is "overlying" the channel region. Usually in the art, "overlie" means, literally, to "lie over." But the floating gate in, for example, Applicant's figure 2, (layer 22) does not lie over the channel region. It lies "next to" the channel region. All of the rest of the floating gates shown in the figures are situated similarly (next to a channel region, rather than over a channel region). Examiner assumes Applicant is using the term "overlie" to encompass a floating gate which is vertically adjacent to the channel controlled by that gate, because this is what is disclosed in the specification. The examiner is not certain, however, that this is the intention.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshida et al. in view of Hsue et al., Sung et al., and Otani et al.

As noted in the previous Office action, the definition of "self-aligned" for this case is taken to be as stated on page 6 of the Board decision of 26 September 2001, i.e., a "self-aligned" floating gate "will not have any horizontal component on the surface of the substrate or on the bottom of the well and therefore will not extend beyond the perimeter of the trench."

With respect to the independent claims, each element of the claims, except the bit line, is clearly shown in the cover figure of Yoshida et al., where the floating gate has no horizontal component on the surface of the substrate or on the bottom of the well, and does not extend beyond the trench perimeter when viewed from above. This meets the definition of "self aligned" as quoted above. In particular, Yoshida layer 12 is an n-type source, layer 10 is a p-type channel (adjacent the floating gate), and layer 7 is an n-type drain. There are therefore "alternating" n and p type layers with a well etched through the layers. Layer 5 is identified as the "word line." See figure 2, which shows that layer 5 is a "line," and column 3, line 33, which states that layer 5 serves as a control gate (which would contact the word line in a memory cell circuit). The bit line of Yoshida et al. is shown as buried bit line 7. Hsue et al. teaches in column 1, lines 49-53, the disadvantages of a buried bit line as compared to a metal bit line overlying the word lines. Hsue et al. figures 2A-2C show the improved bit line as taught by this reference, which overlies the substrate. It would have been obvious to incorporate a bit line such as bit lines "BL" as taught by Hsue et al. in the Yoshida device, in order to gain

the specific advantages noted at column 1, lines 49-53, of the Hsue reference. Such a bit line overlying a word line would necessarily be spaced from the word line by an insulator, to prevent the bit line and the word line from shorting together. Sung et al. and Otani et al. are cited because each of these references also teaches the type of bit line which overlies the substrate. See the cover figure of Sung et al., and, in particular, Otani et al. figure 33 (which shows source layer 24, channel layer 25, drain layer 11, floating gate 20, "self aligned" as this term is defined above, and bit line 16 above the substrate). It would have been obvious to incorporate bit lines as taught by either of these two references in the Yoshida memory device, for the same reason as set forth in Hsue et al. as discussed above. With respect to claim 4, Hsue figure 2C shows bit line BL2 which contacts the top surface of the substrate at all points between the sidewall spacers 57, and is thus "self aligned" to the edge of the sidewall spacers. It would have been obvious to form a similar contact structure in the Yoshida device, because this would give rise to the specific desirable attributes noted above as taught by Hsue et al. A contact to "all points" as shown by Hsue figure 2C would encompass a contact to "at least some points" as recited in claim 5.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to S. Crane, whose telephone number is (703) 308-4894.

The fax phone number for this Group is (703) 308-7722.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist, whose telephone number is (703) 308-0956.

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Sara W Crane
Sara W. Crane
Primary Examiner
Art Unit 2811